

Attorney Docket No. 249930US2S DIV
Inventor: Yoshiaki ASAO
Preliminary Amendment filed: March 10, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-42 (Canceled)

43. (Original) A manufacturing method of a magnetic random access memory, comprising:

forming a first yoke material on an insulating layer on a semiconductor substrate;
forming a conductive material on the first yoke material;
patterning the conductive material and first yoke material;
forming a write line whose lower surface is coated with the first yoke material;
forming a first barrier layer with which the write line is coated;
forming a second yoke material with which the write line is coated on the first barrier layer;
etching the first barrier layer and second yoke material;
leaving the first barrier layer and second yoke material on the side surface of the write line; and
forming a memory cell which uses a magneto resistive effect to store data right on the first write line.

44. (Original) A manufacturing method according to claim 43, further comprising:
forming a second barrier layer between the first yoke material and conductive material.

45. (Original) A manufacturing method according to claim 43, further comprising:

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forming a second barrier layer with which the first yoke material, second yoke material, and write line are coated.

46. (Original) A manufacturing method according to claim 43, wherein the patterning is executed by RIE in which a photoresist is used as a mask.

47. (Original) A manufacturing method according to claim 43, wherein the patterning is executed by RIE in which a silicon insulating layer is used as a mask.

48. (Original) A manufacturing method according to claim 43, wherein the memory cell is formed in a position apart from the write line.

49. (Original) A manufacturing method according to claim 43, wherein the memory cell is formed in a position in contact with the write line.

50. (Original) A manufacturing method of a magnetic random access memory, comprising:

forming a memory cell which uses a magneto resistive effect to store data on an insulating layer on a semiconductor substrate;

forming a conductive material right on the memory cell;

forming a first yoke material on the conductive material;

patterning the first yoke material and conductive material;

forming a write line whose upper surface is coated with the first yoke material;

forming a first barrier layer with which the write line is coated;

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forming a second yoke material with which the write line is coated on the first barrier layer;

etching the first barrier layer and second yoke material; and

leaving the first barrier layer and second yoke material on the side surface of the write line.

51. (Original) A manufacturing method according to claim 50, further comprising:
forming a second barrier layer between the conductive material and first yoke material.

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52. (Original) A manufacturing method according to claim 50, further comprising:
forming a second barrier layer with which the first yoke material, second yoke material, and
write line are coated.

53. (Original) A manufacturing method according to claim 50, wherein the
patterning is executed by RIE in which a photoresist is used as a mask.

54. (Original) A manufacturing method according to claim 50, wherein the
patterning is executed by RIE in which a silicon insulating layer is used as a mask.

55. (Original) A manufacturing method according to claim 50, wherein the memory
cell is formed in a position apart from the write line.

56. (Original) A manufacturing method according to claim 50, wherein the memory
cell is formed in a position in contact with the write line.